§ PATENTEN

1. PATENT：『電流源控制及補償觸控電容感測方法及其裝置』
   PAT NO. I339356 (Taiwan)
   PAT NO. ZL 2007 1 0202087. 0 (CHINA)
2. PATENT：『具環境變化校正的電容式觸控感測裝置』
   PAT NO. M383780 (Taiwan)
   PAT NO. ZL 2010 2 0141537. 7 (CHINA)
3. PATENT：『省電型多鍵觸摸開關感測裝置』
   PAT NO. M375250 (Taiwan)
   PAT NO. ZL 2010 2 0302392. 4 (CHINA)

§ General Description:

TTP258 MCU is an easy-used 4-bit CPU base microcontroller. It contains 1984-word ROM、144-nibble RAM、timer/Counter、interrupt service 、IO control hardware、LVR and touch pad feature for specified applications. The device is also suitable for diverse simple applications in control appliance and consumer product.

§ Features:

1. Tontek RISC 4-bit CPU core
2. Total 26 crucial instructions and two addressing mode
3. Most instructions need 1 word and 1 machine cycle(2 system clocks) except read table instruction(RTB)
4. advance CMOS process
5. Working memory with 1984*16 program ROM and 144*4 SRAM
6. 2-level stacks
7. Operating voltage:
   5.5V~3.1V (LDO ON)；
   5.5V~2.5V (LDO OFF、LVR ON)；
   5.5V~2.2V (LDO OFF、LVR OFF)；
8. System operating frequency: (at VDD=5V)
   . High-speed system oscillator (OSCH):
   ✧ Built-in RC oscillator: 4MHz(typical)
   .Low speed peripheral oscillator (OSCL):
   ✧ Built-in RC oscillator: 16KHz(typical)

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9. Offer 3 IO+10 touch pad or 13 general programmable I/O
    - ✧ IO port built-in key wake-up feature enable by software setting
    - ✧ Providing external interrupt inputs
    - ✧ Offering internal signal outputs, like buzzer(PWM)

10. One 8-bit TCP1 auto-reload timer/counter & one time base counter
    - ✧ 4 timer clock sources selected by software
    - ✧ Time base offers 2 various period interrupt request
11. One 8-bit TCP2 auto-reload timer/counter, can improve PWM function
    - ✧ 4 timer clock sources selected by software
12. Built-in 3 set 8-bit PWM output
13. MCU system protection and power saving controlled mode:
    - ✧ Built-in watch dog timer (WDT) circuit
    - ✧ ROM code error detection
    - ✧ Out of user program's range detection
    - ✧ Providing high/low system operating speed、sleep mode for power saving control
    - ✧ Built-in low voltage reset (LVR) function
14. 10 pins with touch pad detection
15. Built-in LDO voltage 2.7V.
16. Provides 8 interrupt sources
    - ✧ External: INT0, INT1 shared with IO pad
    - ✧ Internal: two Timer/counter, two Time base timer
    - ✧ Two touchpad's interrupt
17. Provide package types
    - ✧ SOP 16/ SOP 8

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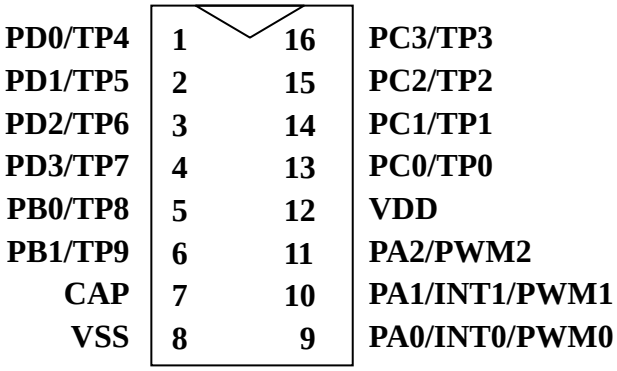
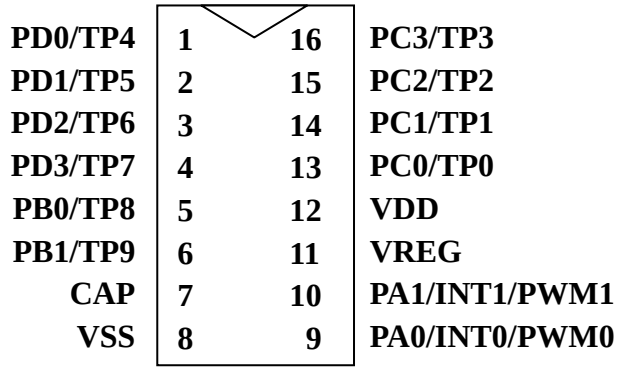
§ Applications:

1. Household electric appliances
2. Consumer products
3. Measurement controller

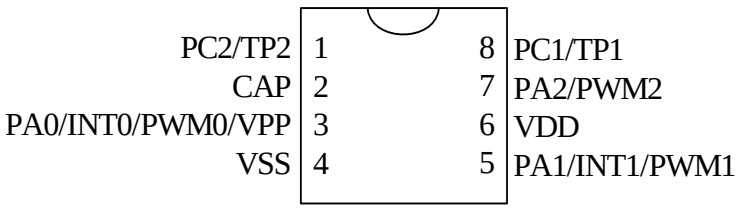
§ Package Description:



TTP258RD-AOB
16-SOP-A
LVRen- by register



TTP258OD-FOB
16-SOP-B
LVRen- Always on



TTP258RD-AO8
8-SOP-A
LVRen- by register

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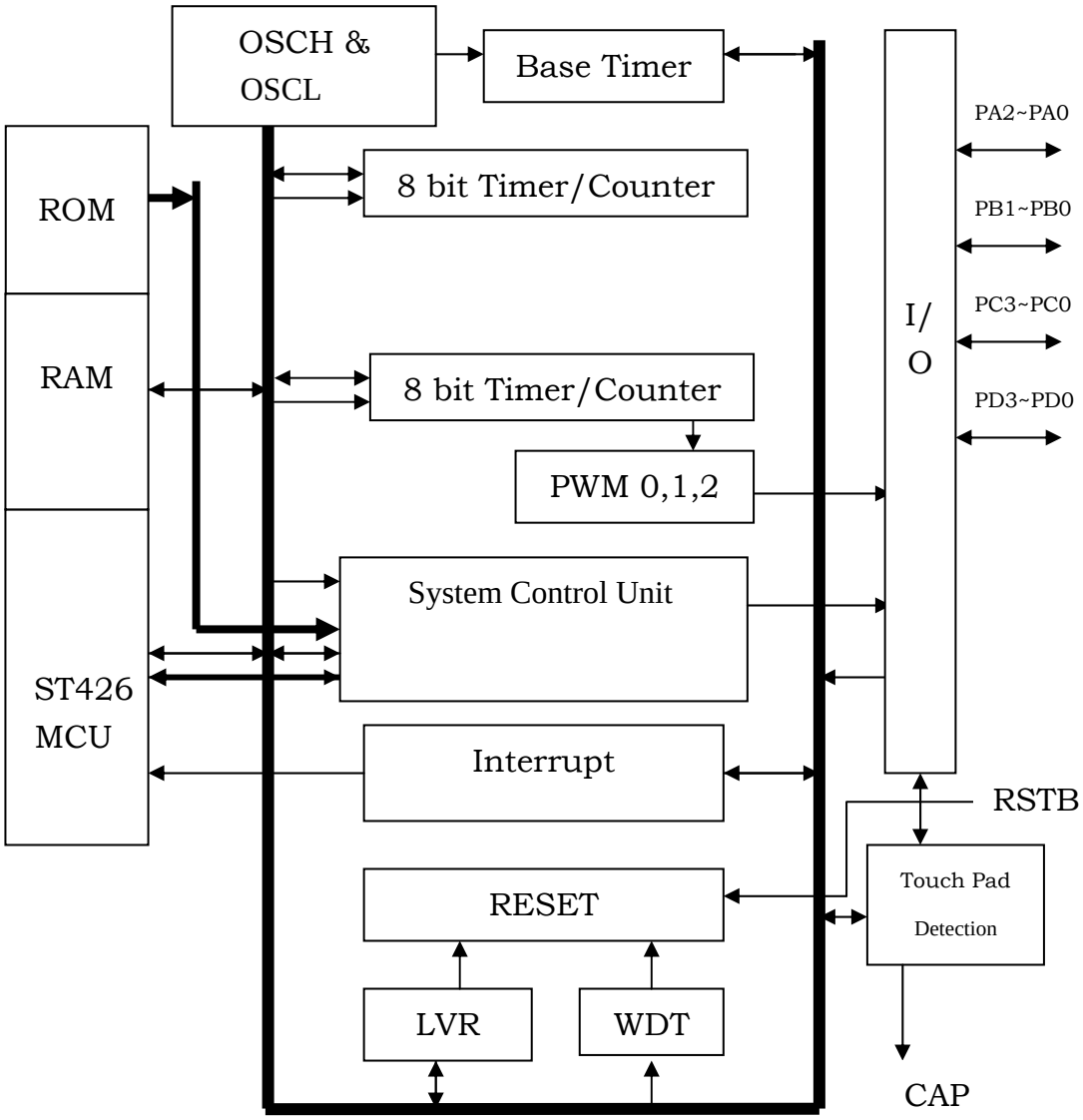
§ Block Diagram:



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§ Pin Description:

Pin Name	Share Pin	I/O	Pin no.	Mask Option	Pin Description
V_{DD}	-	Power	+1	-	Positive power supply
V_{SS}	-	Power	+1	-	Negative power supply, ground
RSTB	-	I	+1	-	External reset input, active low, 50kΩ pull-up(V_{DD} =5v)
PA0 PA1 PA2	INT0/PWM0/VPP INT1/PWM1 PWM2	IO IO IO	+3	-	I/O port with external interrupt input and PWM output (PA0,PA1). PA2 is shared with internal PWM2 output.
PB0 PB1	TP8 TP9	IO/I IO/I	+2	-	IO port or touch pad input.
PC0 PC1 PC2 PC3	TP0 TP1 TP2 TP3	IO/I IO/I IO/I IO/I	+4	-	IO port or touch pad input.
PD0 PD1 PD2 PD3	TP4 TP5 TP6 TP7	IO/I IO/I IO/I IO/I	+4	-	IO port or touch pad input.
CAP	-	O	+1	-	Touch signal output
VREG		Power	+1	-	LDO Voltage output
			18	-	

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§ IO Cell type Description:

Pin Name	I/O Type	Description
PA1	Figure IO-D	STD IO with internal output & external input
PA0	Figure IO-E	STD IO with internal output & external input
PA2	Figure IO-B	STD IO with internal output
PB0~PB1	Figure IO-A	STD IO with external input
PC0~PC3	Figure IO-A	STD IO with external input
PD0~PD3	Figure IO-A	STD IO with external input

§ Absolute Maximum ratings:

ITEM	SYMBOL	RATING	UNIT
Operating Temperature	Top	-20℃ ~ +70℃	℃
Storage Temperature	Tst	-50℃ ~ +125℃	℃
Supply Voltage	VDD	VSS-0.3 ~ VSS+6.0	V
OTP Supply Voltage	VPP	VSS-0.3 ~ VSS+12.5	V
Input Voltage	Vin	VSS -0.3 ~ VDD+0.3	V
Human Body Mode	ESD	>5	KV
Note: VSS symbolizes for system ground			

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DC & AC Characteristics

§ DC Characteristics: (Test condition at room temperature=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDD	F_{OSCH}=4MHz LVR on 2.2V	2.4	-	5.5	V
		LVR off	2.2	-	5.5	
Operating Current (Normal Mode, CPU working, I/O no load)	I_{nd1}	VDD=5.0V, no load, F_{OSCH}=4MHz,	-	2.5	3.0	mA
	I_{nd2}	VDD=5.0V, no load, F_{OSCL} on, F_{OSCH} off, LVR off, LDO off	-	30	50	uA
Operating Current (Sleep Mode, CPU stop, I/O no load)	I_{sd1}	VDD=5.0V, no load, F_{OSCH}=4MHz,	-	0.7	1.0	mA
	I_{sd2}	VDD=3.0V, no load, F_{OSCL} on, F_{OSCH} off, LVR off, LDO off	-	5	10	uA
LVR Current	I_{LVR}	VDD=5.0V	-	55	-	uA
LDO Current	I_{LDO}	VDD=5.0V	-	100	-	uA
Input Ports	V_{IL}	Input Low Voltage	0	-	0.2	VDD
Input Ports	V_{IH}	Input High Voltage	0.8	-	1.0	VDD
RSTB & INT	V_{IL}	Input Low Voltage	0	-	0.3	VDD
RSTB & INT	V_{IH}	Input High Voltage	0.7	-	1.0	VDD
PA0 Sink Current	I_{OL}	VDD=5.0V, VOL=0.6V	-	2	-	mA
PA0 Source Current	I_{OH}	VDD=5V, VOH=VDD-0.7V	-	-1	-	mA
Output port Sink Current (exclude PA0)	I_{OL}	VDD=5.0V, VOL=0.6V	-	8	-	mA
Output Port Source Current (exclude PA0)	I_{OH}	VDD=5V, VOH=VDD-0.7V	-	-4	-	mA
I/O Port Pull-up Resistor	R_{PH}	VDD=5.0V	100	150	200	KΩ
RSTB Pull-up Resistor	R_{PH}	VDD=5.0V	30	50	80	KΩ
Low Voltage Reset (LVR)	V_{LVR1}	LVR select 2.2V	2.0	2.2	2.4	V
LDO Voltage	V_{LDO1}	LDO select 2.7V	2.4	2.7	3.0	V
Bandgap Voltage	V_{BGAP}		1.0	1.12	1.23	V

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§ AC Characteristics:

Parameter	Test Condition		Min.	Typ.	Max.	Unit
External Reset	Low active pulse width tRES		2	-	-	CPU clock
Interrupt input	Low active pulse width tINT		2	-	-	
Wake up input	Low active pulse width $t_{wkup,}$ Application de-bounce should be manipulated by user' software		2	-	-	OSCL
System Oscillator Frequency	F_{OSCH} (Built-in RC)	VDD=5.0V	-	4M	-	Hz
Peripheral Oscillator Frequency	Built-in F_{OSCL}(RC)	VDD=2.2~5.0V	-	16K	-	Hz
Startup Period of Oscillators	T_{OSCH} (Built-in RC)	wake-up from off mode	8	-	-	F_{OSCH}
	T_{OSCL} (Built-in RC)	Wake-up from off mode	8	-	-	F_{OSCL}
Stable Time Of System Clock Switching	T_{OSCH} (Built-in RC)	OSCL→OSCH & OSCH off	8	-	-	F_{OSCH}
	(If H/L=0 then OSCH stop)					
	T_{OSCL} (Built-in RC)	OSCH→OSCL & OSCL on	8	-	-	F_{OSCL}
Timer/Counter input clock frequency	Input frequency rating, no de-bounce circuit built-in ,at VDD=5V		DC	-	4M	Hz
System Stable Time after Power up	After power up, the system needs to initialize the configured state and OST.		-	-	40	ms

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§ Memory Map:

ROM ADDRESS	RAM ADDRESS	Function Block
000_H~$7BF_H$	-	Program ROM [1984*16]
-	000_H ~007_H	File Registers
-	008_H~$01F_H$	Peripheral registers (I)
-	020_H~$0AF_H$	Working RAM [144*4]
-	200_H~304_H	Peripheral registers (II)

§ Interrupt Vectors:

Interrupt Vectors	Function Description
$000	hardware RESET
$001	Hardware IRQ

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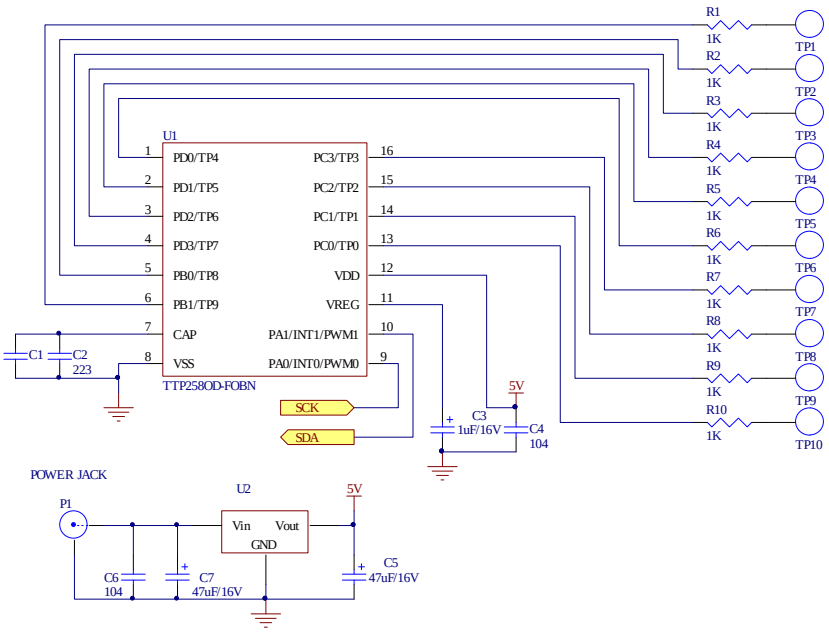
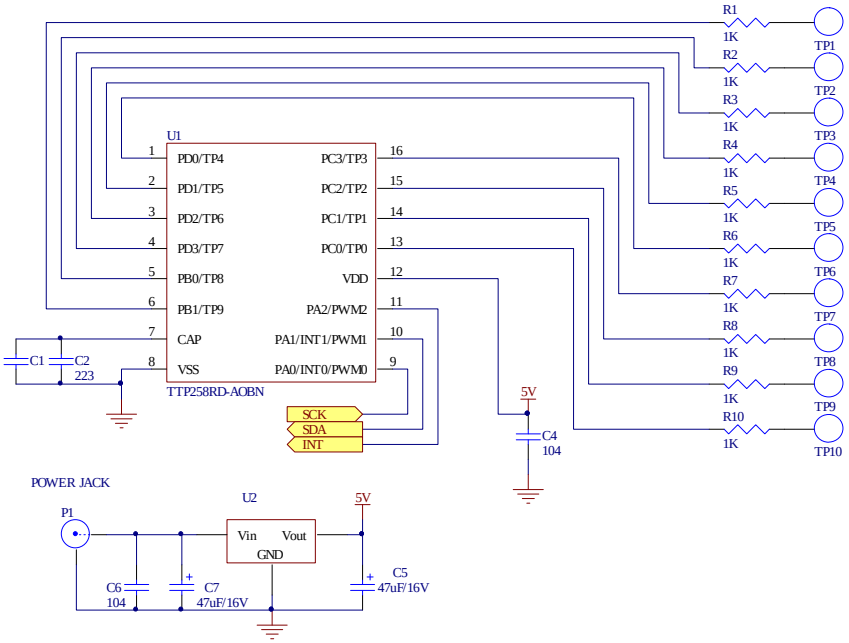
§ Application Circuit

10 KEYS SPI 串列輸出(二線式)



10 KEYS SPI 串列輸出(二線或三線式)



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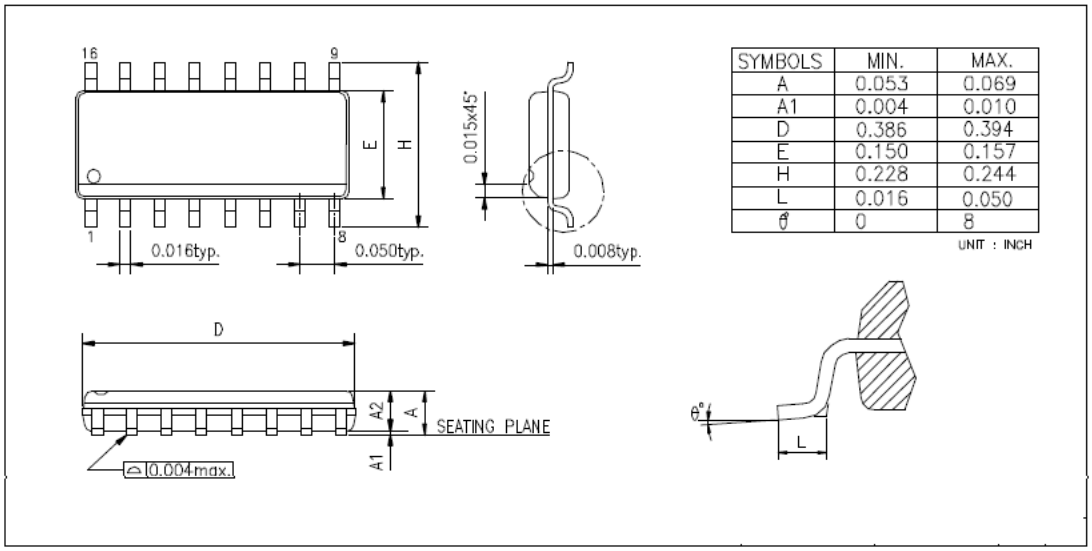
§ Package & PAD Information:

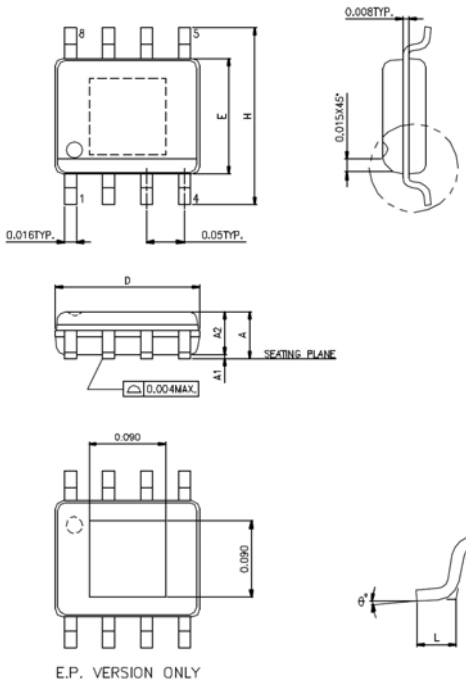
(16-SOP)



SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
D	0.386	0.394
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

- **SOP 8**



SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
A2	–	0.059
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1.JEDEC OUTLINE : MS-012 AA / E.P. VERSION : N/A
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

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§ Ordering Form:

	Package type	LVRen	LVR	LDO
TTP258RD-AOBN	**16-SOP-A**	By Register	2.2V	2.7V
TTP258OD-FOBN	**16-SOP-B**	Always on	2.2V	2.7V
TTP258RD-AO8N	**8-SOP-A**	By Register	2.2V	2.7V

Modified Record:

Body:

2014/05/28

- New build

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